Amendments to the Claims

Please amend the claims as follows:

1-100. (canceled)

101. (withdrawn) A transistor in a semiconductor device, comprising:

source/drain diffusion regions formed on a semiconductive region of a substrate; and

a transistor gate formed on the semiconductive region between the source/drain diffusion regions, the transistor gate extending in a vertical orientation from the substrate, the transistor gate comprising at least two overlying layers of epitaxial silicon, including an uppermost epitaxial layer;

each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial silicon layer having an insulated top surface.

102. (withdrawn) The transistor of Claim 101, wherein the source/drain diffusion regions are elevated and extend in a vertical orientation from the substrate surface adjacent to the transistor gate.

103. (withdrawn) The transistor of Claim 102, wherein each of the source/drain diffusion regions comprise at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface, and insulated sidewalls, and an uppermost epitaxial silicon layer having an insulated top surface.

104. (withdrawn) The transistor of Claim 103, wherein the uppermost epitaxial silicon layer of the source/drain diffusion regions comprise a conductivity enhancing dopant.

105. (withdrawn) The transistor of Claim 103, wherein each of the epitaxial silicon layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

106. (withdrawn) The transistor of Claim 101, wherein each epitaxial silicon layer comprises a faceted top surface.

107. (withdrawn) The transistor of Claim 101, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

108. (withdrawn) The transistor of Claim 101, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

109. (withdrawn) The method of Claim 108, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

110. (withdrawn) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

elevated source/drain diffusion regions disposed on the semiconductive region adjacent to the transistor gate, and extending in a vertical plane from the substrate;

each of the source/drain diffusion regions comprising at least two overlying layers of epitaxial silicon, including an uppermost epitaxial silicon layer; each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial silicon layer having an insulated top surface.

111. (withdrawn) The transistor of Claim 110, wherein the source/drain diffusion regions comprise an uppermost epitaxial silicon layer comprising a conductivity enhancing dopant.

112. (withdrawn) The transistor of Claim 110, wherein at least one of the epitaxial silicon layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

113. (withdrawn) The transistor of Claim 112, wherein at least one of the epitaxial silicon layers comprises a concentration gradient of the dopant.

114. (withdrawn) The transistor of Claim 110, wherein the epitaxial silicon layers comprise a faceted top surface.

115. (withdrawn) The transistor of Claim 110, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

116. (withdrawn) The transistor of Claim 110, wherein the transistor gate is covered by a layer of insulative material and comprises at least two overlying layers of epitaxial silicon.

117-122. (canceled)

123. (withdrawn) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

an elevated source/drain diffusion region disposed on the substrate adjacent to the transistor gate in a vertical orientation from the substrate; the source/drain diffusion region comprising at least two overlying layers of epitaxial silicon, including an uppermost epitaxial layer; each of the at least two epitaxial silicon layers comprising a top surface and sidewalls, with a layer of an insulative material disposed over the sidewalls; and the uppermost epitaxial layer having a top surface with an overlying layer of an insulative material.

124. (withdrawn) The transistor of Claim 123, wherein at least one of the epitaxial silicon layers of the source/drain diffusion region comprises a conductivity enhancing dopant.

125. (withdrawn) The transistor of Claim 124, wherein the uppermost epitaxial silicon layer of the source/drain diffusion region comprises a conductivity enhancing dopant.

126. (withdrawn) The transistor of Claim 124, wherein at least one of the epitaxial silicon layers comprises a concentration gradient of the dopant.

127. (withdrawn) The transistor of Claim 124, wherein the conductivity enhancing dopant comprises a p-type dopant.

128. (withdrawn) The transistor of Claim 124, wherein the conductivity enhancing dopant comprises an n-type dopant.

129. (withdrawn) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, including an uppermost epitaxial layer; each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

130. (withdrawn) The semiconductor structure of Claim 129, wherein each epitaxial silicon layer comprises a top surface defining a facet.

131. (withdrawn) The semiconductor structure of Claim 129, wherein the facet has a (100) plane orientation.

132. (withdrawn) The semiconductor structure of Claim 129, wherein each epitaxial silicon layer has a thickness of up to about 200 nm.

133. (withdrawn) The semiconductor structure of Claim 132, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

134. (withdrawn) The semiconductor structure of Claim 132, wherein one or more epitaxial silicon layers has a thickness of about 70 to about 100 nm.

135. (withdrawn) The semiconductor structure of Claim 132, wherein each epitaxial silicon layer has a thickness of at least about 10 nm to about 30 nm.

136. (withdrawn) The semiconductor structure of Claim 129, being disposed adjacent to a gate or word line.

137. (withdrawn) The semiconductor structure of Claim 129, being disposed adjacent to a source/drain region.

138. (withdrawn) The semiconductor structure of Claim 137, being a transistor gate.

139. (withdrawn) The semiconductor structure of Claim 138, wherein the transistor gate is isolated within the substrate by at least one dielectric isolation region disposed in the substrate adjacent thereto.

140. (withdrawn) The semiconductor structure of Claim 129, being a source/drain diffusion region.

141. (withdrawn) The semiconductor structure of Claim 140, wherein the uppermost epitaxial silicon layer comprises a conductivity enhancing dopant.

142. (withdrawn) The semiconductor structure of Claim 140, wherein each of the epitaxial silicon layers comprises a conductivity enhancing dopant.

143. (**currently amended**) A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface and sidewalls, and insulative material over the sidewalls, the top surface defining a facet; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface; wherein the structure is disposed on a substrate in a vertical orientation.

144. (previously presented) The semiconductor structure of Claim 143, wherein the insulative layer comprises an oxide film, a nitride film, an oxidized nitride film, or a composite oxide/nitride film.

145. (previously presented) The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon nitride film.

146. (previously presented) The semiconductor structure of Claim 145, wherein the silicon nitride film has a thickness of about 5 to about 20 nm.

147. (previously presented) The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon oxide film.

148. (previously presented) The semiconductor structure of Claim 147, wherein the silicon oxide film has a thickness of about 2 to about 5 nm.

149. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface, sidewalls, and an insulative material over the sidewalls, the top surface defining a facet; an uppermost epitaxial ~~layer~~ silicon crystal of the at least two overlying ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface; one or more of the epitaxial silicon ~~layers~~ crystals comprising a conductivity enhancing dopant; wherein the structure is disposed on a substrate in a vertical orientation.

150. (previously presented) The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises a p-type dopant.

151. (previously presented) The semiconductor structure of Claim 150, wherein the p-type dopant is selected from the group consisting of diborane, boron trichloride, and boron trifluoride, and combinations thereof.

152. (previously presented) The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises an n-type dopant.

153. (previously presented) The semiconductor structure of Claim 152, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

154. **(currently amended)** The semiconductor structure of Claim 149, wherein one or more of the epitaxial ~~layers~~ silicon crystals comprises a concentration gradient of the dopant ~~within the epitaxial layer~~.

155. **(currently amended)** The semiconductor structure of Claim 154, wherein the concentration gradient comprises a low to high concentration of the dopant within the epitaxial ~~layer~~ silicon crystal, with the high dopant concentration at the top surface of ~~the layer~~ said crystal.

156. (withdrawn) The semiconductor structure of Claim 129, being a component of a transistor.

157. (withdrawn) The semiconductor structure of Claim 156, being a transistor gate.

158. (withdrawn) The semiconductor structure of Claim 156, being a source/drain diffusion region.

159. (withdrawn) The semiconductor structure of Claim 158, wherein at least one of the epitaxial layers of the source/drain diffusion regions comprises a conductivity enhancing dopant.

160. (withdrawn) The semiconductor structure of Claim 159, wherein at least one of the epitaxial silicon layers of the source/drain diffusion regions comprises a concentration gradient of a conductivity enhancing dopant.

161. (withdrawn) The semiconductor structure of Claim 157, wherein the transistor gate is disposed over a drain region disposed in the substrate.

162. (withdrawn) The semiconductor structure of Claim 161, the drain region is about 50 nm to about 100 nm wide.

163. (withdrawn) The semiconductor structure of Claim 161, wherein the uppermost epitaxial silicon layer of the transistor gate structure comprises a source region doped with a conductivity enhancing dopant.

164. (withdrawn) The semiconductor structure of Claim 163, wherein the uppermost epitaxial silicon layer is at least about 10 nm thick.

165. (withdrawn) The semiconductor structure of Claim 156, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

166. (withdrawn) The semiconductor structure of Claim 165, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

167. (previously presented) The semiconductor structure of Claim 143, being a component of a transistor.

168. (previously presented) The semiconductor structure of Claim 167, being a transistor gate.

169. (previously presented) The semiconductor structure of Claim 167, being a source/drain diffusion region.

170. (previously presented) The semiconductor structure of Claim 149, being a component of a transistor.

171. (previously presented) The semiconductor structure of Claim 170, being a transistor gate.

172. (previously presented) The semiconductor structure of Claim 170, being a source/drain diffusion region.

173. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal comprising a top surface and insulated sidewalls, the top surface defining a facet, and the uppermost epitaxial silicon ~~layer~~ crystal having an insulated top surface; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

174. (previously presented) The semiconductor structure of Claim 173, being a transistor gate.

175. (previously presented) The semiconductor structure of Claim 173, being a source/drain diffusion region.

176. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface, sidewalls, and insulative material over the sidewalls, the top surface defining a facet; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying ~~layer~~ silicon crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

177. (previously presented) The semiconductor structure of Claim 176, being a transistor gate.

178. (previously presented) The semiconductor structure of Claim 176, being a source/drain diffusion region.

179. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon layer comprising a top surface, sidewalls, and insulative material over the sidewalls, the top surface defining a facet; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface; one or more of the at least two epitaxial silicon ~~layers~~ crystals comprising a conductivity enhancing dopant; the structure disposed on a substrate in a vertical orientation; and the structure being a component of a transistor.

180. (previously presented) The semiconductor structure of Claim 179, being a transistor gate.

181. (previously presented) The semiconductor structure of Claim 179, being a source/drain diffusion region.

182. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface and insulated sidewalls with the top surface defining a facet, and an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

183. (previously presented) The semiconductor device of Claim 182, comprising a transistor.

184. (previously presented) The semiconductor device of Claim 183, wherein the structure comprises a transistor gate.

185. (previously presented) The semiconductor device of Claim 183, wherein the structure comprises a source/drain diffusion region.

186. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface and sidewalls with the top surface defining a facet, and insulative material over the sidewalls; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface; and the structure disposed on a substrate in a vertical orientation.

187. (previously presented) The semiconductor device of Claim 186, comprising a transistor.

188. (previously presented) The semiconductor device of Claim 187, wherein the structure comprises a transistor gate.

189. (previously presented) The semiconductor device of Claim 187, wherein the structure comprises a source/drain diffusion region.

190. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface and sidewalls, with the top surface defining a facet and insulative material over the sidewalls; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface; one or more of the at least two epitaxial silicon ~~layers~~ crystals comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

191. (previously presented) The semiconductor device of Claim 190, comprising a transistor.

192. (previously presented) The semiconductor device of Claim 191, wherein the structure comprises a transistor gate.

193. (previously presented) The semiconductor device of Claim 191, wherein the structure comprises a source/drain diffusion region.

194. (withdrawn) A transistor in a semiconductor device, comprising:

source/drain diffusion regions disposed on a semiconductive region of a substrate; and

a transistor gate disposed on the semiconductive region between the source/drain diffusion regions, the transistor gate comprising two or more overlying layers of epitaxial silicon extending in a vertical orientation from the substrate, each epitaxial silicon layer comprising a top surface and insulated sidewalls; wherein a first epitaxial silicon layer is disposed on the substrate, and a second epitaxial silicon layer is disposed on the top surface of the first epitaxial silicon layer; and an uppermost epitaxial silicon layer of the transistor gate comprises an insulated top surface.

195. (withdrawn) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

an elevated source/drain diffusion region disposed on the substrate adjacent to the transistor gate in a vertical orientation from the substrate; the source/drain diffusion region comprising at least two overlying layers of epitaxial silicon including an uppermost epitaxial layer; each of the at least two epitaxial silicon layers comprising a top surface, sidewalls, and insulative spacers over the sidewalls; and the uppermost epitaxial layer having a top surface with an overlying layer of an insulative material.

196. (**currently amended**) A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each of the at least two epitaxial silicon ~~layers~~ crystals having a top surface, sidewalls, ~~and~~ insulative spacers over the sidewalls, and the top surface defining a facet; an uppermost epitaxial ~~layer~~ crystal having a ~~top surface with an overlying~~ layer of an insulative material over the top surface; one or more of the at least

two epitaxial silicon ~~layers~~ crystals comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

197. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface, sidewalls, ~~and~~ insulative material along the sidewalls, and the top surface defining a facet; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface of said crystal; and the structure disposed on a substrate in a vertical orientation.

198. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface defining a facet, and insulated sidewalls; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface of said crystal; one or more of the epitaxial silicon ~~layers~~ crystals comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

199. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal having a top surface defining a facet, sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial silicon ~~layer~~ crystal having a ~~top surface with an overlying~~ layer of an insulative material over the top surface of said crystal; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

200. **(currently amended)** A semiconductor structure, comprising:

at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal having a top surface defining a facet, sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial silicon ~~layer~~ crystal having a ~~top surface with an overlying~~ layer of an

insulative material over the top surface of said crystal; one or more of the at least two overlying ~~layers of~~ epitaxial silicon crystals comprising a conductivity enhancing dopant; the structure disposed on a substrate in a vertical orientation; and the structure being a component of a transistor.

201. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal having a top surface and insulated sidewalls, the top surface defining a facet; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface of said uppermost silicon crystal; and the structure disposed on a substrate in a vertical orientation.

202. **(currently amended)** A semiconductor device, comprising:

a structure comprising at least two overlying ~~layers~~ crystals of epitaxial silicon, each epitaxial silicon ~~layer~~ crystal comprising a top surface defining a facet, and sidewalls covered by an insulative material; an uppermost epitaxial silicon ~~layer~~ crystal of the at least two overlying epitaxial silicon ~~layers~~ crystals having a ~~top surface with an overlying~~ layer of an insulative material over the top surface of said uppermost silicon crystal; one or more of the epitaxial silicon ~~layers~~ crystals comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

203. **(currently amended)** A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on the substrate; the first epitaxial silicon ~~layer~~ crystal comprising sidewalls, and a top surface defining a facet;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon ~~layer~~ crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial silicon ~~layer~~ crystal, the second epitaxial silicon ~~layer~~ crystal comprising sidewalls and a top surface defining a facet; and

depositing an insulative material layer thereover.

204. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, and insulative material disposed on the sidewalls, the top surface of said crystals defining a facet, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial ~~layer~~ silicon crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial ~~layer~~ silicon crystal;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial ~~layer~~ silicon crystal;

repeating the steps of selectively growing an epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein, upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

205. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls,

and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, depositing an insulative film over the underlying epitaxial ~~layers~~ silicon crystals, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

206. (**currently amended**) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layer~~ crystal of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, depositing an oxide film and removing a portion of the oxide film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an oxide film layer thereover, with no subsequent removal of the oxide film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

207. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, depositing a nitride film and removing a portion of the nitride film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing a nitride film layer thereover, with no subsequent removal of the nitride film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

208. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate to about 450°C to about 950°C., and flowing at least one silicon precursor gas over the substrate at a rate of about 10 sccm to about 500 sccm, for about 15 seconds to about 30 seconds;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, depositing an insulative film over the underlying epitaxial ~~layers~~ silicon crystals, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and

selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

209. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial ~~layer~~ silicon crystal at about 20 nm/minute to about 40 nm/minute;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, depositing an insulative film over the underlying epitaxial ~~layers~~ silicon crystals, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

210. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls,

and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial ~~layer~~ silicon crystal of less than about 10 nm/minute;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, depositing an insulative film over the underlying epitaxial ~~layers~~ silicon crystals, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

211. (**currently amended**) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal oxidation, with no

subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

212. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

213. **(currently amended)** A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on the substrate; the first epitaxial silicon ~~layer~~ crystal comprising sidewalls, and a top surface defining a facet;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon ~~layer~~ crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial silicon ~~layer~~ crystal while depositing a conductivity enhancing dopant, the second epitaxial silicon ~~layer~~ crystal comprising sidewalls, and a top surface defining a facet;

depositing an insulative material layer thereover.

214. **(currently amended)** A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on the substrate; the first epitaxial silicon ~~layer~~ crystal comprising sidewalls, and a top surface defining a facet;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon ~~layer~~ crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial silicon ~~layer~~ crystal, the second epitaxial silicon ~~layer~~ crystal comprising sidewalls, and a top surface defining a facet;

doping the second epitaxial ~~layer~~ silicon crystal with a conductivity enhancing dopant by ion implantation, and

depositing an insulative material layer thereover.

215. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial ~~layer~~ silicon crystal at about 20 nm/minute to about 40 nm/minute, wherein selectively growing at least the

uppermost epitaxial ~~layer~~ silicon crystal comprises flowing the at least one silicon precursor gas with a conductivity enhancing dopant over the substrate; and

prior to selectively growing each epitaxial silicon ~~layer~~ crystal, depositing an insulative film over the underlying epitaxial ~~layers~~ silicon crystals, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and,

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

216. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial ~~layer~~ silicon crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial ~~layer~~ silicon crystal;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial ~~layer~~ silicon crystal; and

repeating the steps of selectively growing an epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial ~~layer~~ silicon crystal,

depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial ~~layer~~ silicon crystal;

wherein, upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

217. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial ~~layer~~ silicon crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial ~~layer~~ silicon crystal;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial ~~layer~~ silicon crystal; and

repeating the steps of selectively growing an epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial ~~layer~~ silicon crystal, depositing a conductivity enhancing dopant at a variable rate to provide a concentration gradient of the dopant within the uppermost epitaxial ~~layer~~ silicon crystal;

wherein, upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

218. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a crystal and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial ~~layer~~ silicon crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial ~~layer~~ silicon crystal;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial ~~layer~~ silicon crystal; and

repeating the steps of selectively growing an epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial ~~layer~~ silicon crystal, depositing a conductivity enhancing dopant at an increasing rate over time to provide a low to high concentration of the dopant within the uppermost epitaxial ~~layer~~ silicon crystal;

wherein, upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

219. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial ~~layer~~ silicon crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial ~~layer~~ silicon crystal;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial ~~layer~~ silicon crystal; and

repeating the steps of selectively growing an epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein the uppermost epitaxial ~~layer~~ silicon crystal is selectively grown while doping, and upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

220. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial ~~layer~~ silicon crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial ~~layer~~ silicon crystal;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial ~~layer~~ silicon crystal; and

repeating the steps of selectively growing an epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure;

wherein, upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, doping the uppermost epitaxial ~~layer~~ silicon crystal with a conductivity enhancing dopant by ion implantation, and depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

221. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and, during the step of selectively growing the uppermost epitaxial ~~layer~~ silicon crystal, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial ~~layer~~ silicon crystal; and

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

222. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying ~~layers~~ crystals of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial ~~layer~~ silicon crystal, and selectively growing the epitaxial silicon ~~layer~~ crystal on the exposed top surface of the preceding epitaxial ~~layer~~ silicon crystal; and, during the step of selectively growing the uppermost epitaxial ~~layer~~ silicon crystal, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial ~~layer~~ silicon crystal; and

upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, forming an insulative film over the epitaxial ~~layers~~ silicon crystals by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

223. **(currently amended)** A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying ~~layers~~ crystals of epitaxial silicon including an uppermost epitaxial silicon ~~layer~~ crystal; each epitaxial silicon ~~layer~~ crystal having a top surface and sidewalls, the top surface defining a facet and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon ~~layer~~ crystal comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon ~~layer~~ crystal on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial ~~layer~~ silicon crystal;

selectively growing a second epitaxial silicon ~~layer~~ crystal on the exposed top surface of the first epitaxial ~~layer~~ silicon crystal;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial ~~layer~~ silicon crystal; and

repeating the steps of selectively growing an epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial ~~layer~~ silicon crystal, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial ~~layer~~ silicon crystal;

wherein, upon selectively growing the uppermost epitaxial silicon ~~layer~~ crystal, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon ~~layer~~ crystal.

224. **(new)** The semiconductor structure of Claim 143, wherein the top surface of at least one of said epitaxial silicon crystals defines a facet having a (100) plane orientation.

Supplemental Information Disclosure Statement.

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, Applicant submits the information listed on the enclosed Form 1449/PTO for consideration in the above-identified application. No representation is made that a reference is "prior art" within the meaning of 35 U.S.C. §§ 102/103.

The references listed on the Form PTO 1449 were submitted in the parent application **USSN 09/816,962**. Accordingly, a copy of these documents is not provided because these documents are available in the co-pending parent application. However, if these references are not available to the Examiner, Applicant will provide a copy upon request.

This Supplemental Information Disclosure Statement is being filed after the mailing of a final action and before a Notice of Allowance. Accordingly, please charge the necessary fee for the consideration of these references to Account No. 23-2053.

Consideration of the listed references is requested, and return of the enclosed Form 1449/PTO is requested showing the items as being initialed and considered.

The Form 1449/PTO is attached hereto at the **Appendix**.